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VERIGY ASILEIM TECHNOLOGIES, INC. Legal Department, DL429 Intellectual Property Administration P. O. Box 7599

ATTORNEY DOCKET NO. 10031350-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Hildebrant

Loveland, Colorado 80537-0599

Serial No.: 10/815,521 Examiner: Doan, Njhla M

Filing Date: April 1, 2004

Group Art Unit: 2825

Title: VERIFICATION OF INTEGRATED CIRCUIT TESTS USING TEST SIMULATION AND

INTEGRATED CIRCUIT SIMULATION WITH SIMULATED FAILURE

COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:								
Transmitted herewith is/are the following in the above-identified application:								
×	Response/Amendment			Petition to extend time to respond				
	New fee as calculated below			Supplemental Declaration				
×	No additional fee (Address envelope to "Mail Stop Amendments")							
	Other: (Fee \$)							
	CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY							
Ī	(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE		(7) ITIONAL EES
-	TOTAL	30	MINUS	37	= 0	X 50	\$	0
+	INDEP.	3	MINUS	3	= 0	X 200	\$	0
}	CLAIMS + 360						\$	0
-	EXTENSION 18T MONTH		2 ND MONTH 3 RD MONTH 4 ^{TI}		4 TH M 1590	ONTH	\$	0
L	FEE	120.00	450.00	1020.00		HER FEES	\$	
	TOTAL ADDITIONAL FEE FOR THIS AMEND						- \$	0

to Deposit Account 50-1078. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 50-1078 pursuant to 37 CFR 1.2 5. Additionally please charge any fees to Deposit Account 50-1078 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Hildebrant

I hereby cartify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below:

Date of facsimile: 07-06-2006

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Rev 06/05 (TrensAmd)

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

PATENT APPLICATION: Serial No. 10/815,521

ORIGINALLY FILED: April 1, 2004

FOR: VERIFICATION OF INTEGRATED CIRCUIT TESTS USING TEST SIMULATION AND INTEGRATED CIRCUIT SIMULATION WITH SIMULATED FAILURE

INVENTOR: Hildebrant, Andrew

GROUP ART UNIT: 2825

EXAMINER: Doan, Nghia M

DOCKET NUMBER: 10031350-1

SUPPLEMENTARY AMENDMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed January 26, 2006, please amend the above-identified patent application and consider the remarks as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.